the action of electromagnetic radiation in the infrared range of wavelength longer than 1 μm.--

IN THE SPECIFICATION:

Page 1, between the title and first full paragraph, insert the following:

--This application is a U.S. National Phase Application under 35 USC 371 of International Application PCT/FR99/02428 (not published in English) filed October 8, 1999.--

--FIELD OF THE INVENTION--;

between lines 5 and 6, insert the following heading:

--BACKGROUND OF THE INVENTION--.

Page 2, between lines 22 and 23, insert the following heading:

--SUMMARY OF THE INVENTION--.

Page 2, line 23 through page 3, line 2, replace as follows:

--One object of the invention is to provide a semiconductor chip for a chip-containing portable article, which chip is not sensitive to the action of electromagnetic radiation in the ultraviolet, visible and infrared ranges.

A5 According to one aspect of the invention, the chip comprises a silicon substrate layer whose active face has circuits integrated therein defining a central processor unit and memories. The chip further comprises physical means for providing physical protection against the action of electromagnetic radiation in the infrared range at a wavelength longer than 1 μm. For example, an additional layer of silicon covers at least part of the active face.

Page 3, between lines 6 and 7, insert the following header:

A6 --BRIEF DESCRIPTION OF THE DRAWINGS--.

Page 3, lines 16-18, replace as follows:

--Figure 4A is one variation of a cross section taken along line 4A-4A of Figure 3B;

A7 Figure 4B is a cross section taken along line 4B-4B of Figure 3A;

Figure 4C is another variation of a cross section taken along line 4A-4A of Figure 3B;--

Page 3, lines 22-27, replace as follows:

--Figure 6A is a variant of a second embodiment taken along a cross section similar to that of Figure 4A;

Figure 6B is a second embodiment taken along a cross section similar to Figure 4B;

Figure 6C is another variant of the second embodiment as shown in Figure 6A;

Figure 6D is yet another variant of the second embodiment as shown in Figure 6A;

Figure 7A is a variant of a third embodiment taken along a cross section similar to that of Figure 4A;

Figure 7B is a third embodiment taken along a cross section similar to Figure 4B;

Figure 7C is another variant of the third embodiment as shown in Figure 7A; and

Figure 7D is yet another variant of the third embodiment as shown in Figure 7A.--

Page 3, between lines 27 and 28, insert the following heading:

--DETAILED DESCRIPTION OF THE DRAWINGS--.

Page 4, line 30 through page 5, line 10, replace as follows:

--In a second type of chip 5a shown in Figure 3B (and one variation thereof shown in Figure 4A), the chip 5a has in similar

manner a silicon substrate layer 12a whose thickness has been reduced and is therefore thinner than the silicon substrate layer 12 shown in Figure 3A. This silicon substrate layer 12a likewise has an active face 13a which includes the integrated circuits and a face opposite said active face, i.e. the rear face 6a. However, the active face 13a is covered in an additional layer 14 of silicon which is sealed to said face 13a via a sealing layer 15. The additional layer 14 has a top face 18 and a bottom face 19 in contact with the sealing layer. The sealing layer 15 and the additional layer 14 advantageously cover all or at least a major portion of the active face 13a of the chip 5a with the exception of the contact pads 8a which remain accessible through openings 16, or "vias", formed through said layers 14 and 15. In practice, the thicknesses of the various layers are as follows. Thinned substrate layer: about 15 $\mu$m; additional layer: about 150 $\mu$m; and sealing layer: about 10 $\mu$m.--

Page 6, lines 25-36, replace as follows:

--The dopants 17 can be present in the silicon substrate layer 12 of a chip 5 of the first type or of a chip 5a of the second type. They can also be incorporated in the additional layer 14 of a chip 5a of the second type.

In the variant of Figure 4A which shows a chip 5a of the second type, the dopants 17 are present in the additional layer 14 of the chip 5a. They are uniformly distributed throughout

this layer 14. Nevertheless, they could be concentrated solely in a fraction of the thickness of said layer 14, in particular in the portion of said layer that is close to its top face 18.--

Page 7, lines 8-19, replace as follows:

--In the variant of Figure 4C which shows a chip 5a of the second type, the dopants 17 are present both in the substrate layer 12a of the chip and in its additional layer 14.

In a second embodiment of the invention as shown in Figures 6A, 6B, 6C and 6D the means providing physical protection against the action of light are formed by surface irregularities 20 visible on a face of a layer of silicon. These surface irregularities can be visible on the rear face of the silicon substrate or on one or two of the top and bottom faces of the additional layer 14 for chips 5a of the second type.--

Page 8, lines 3-22, replace as follows:

--In the variant of Figure 6A which shows a chip 5a of the second type, the irregularities 20 are formed on the face of the additional layer 14 which comes into contact with the sealing layer 15.

In the variant of Figure 6B which shows a chip 5 of the first type, the irregularities 20 are formed in the rear face of the silicon substrate layer.

In the variant of Figure 6C which shows a chip 5a of the second type, the irregularities 20 are formed in the face 18 of the additional layer.

In the variant of Figure 6D which shows a chip 5a of the second type, the irregularities 20 are formed in the top face 18 of the additional layer 14, in its bottom face 19, and in the rear face 6a of the chip 5a.

In a third embodiment of the invention shown in Figures 7A, 7B, 7C and 7D, the physical protection means are formed by a metal layer 21 assembled on at least one of the faces of the substrate or additional layers 12 or 14 of silicon and having a thickness of more than 50 Ångstroms (Å), e.g. about 100 Å.--

Page 9, lines 1-11, replace as follows:

In the variant of Figure 7B which shows a chip 5 of the first type, the metal layer 21 is placed on the rear face of the substrate layer 12.

In the variant of Figure 7C which shows a chip 5a of the second type, the metal layer 21 is placed on the top face 18 of the additional layer 14.

In the variant of Figure 7D which shows a chip 5a of the second type, a first metal layer is placed between the additional layer 14 and the sealing layer 15, and a second metal layer is placed on the rear face of the substrate layer 12a.--